CLAIMS

What is claimed is:

1. A semiconductor device formed on a semiconductor substrate having an active region, the semiconductor device comprising:

a dielectric layer interposed between a gate electrode and the semiconductor substrate; and

graded dielectric constant spacers formed on sidewalls of the dielectric layer, sidewalls of the gate electrode and portions of an upper surface of the semiconductor substrate,

wherein the dielectric constant of the graded dielectric constant spacers decreases in a direction away from the sidewalls of the dielectric layer.

2. A semiconductor device according to claim 1, wherein the graded dielectric constant spacers comprising:

a first layer formed on the sidewalls of a gate electrode, the sidewalls of the dielectric layer and the portions of the upper surface of the semiconductor substrate;

a second layer formed on the first layer;

a third layer formed on the second layer; and

a fourth layer formed on the third layer,

wherein the first layer has a dielectric constant greater than SiO_2 and each of the second, third and fourth layers has a dielectric constant less than the dielectric constant of the preceding layer.

3. A semiconductor device according to claim 1, wherein the graded dielectric constant spacers further comprise:

recessed spacers formed on the sidewalls of the dielectric layer, portions of an upper surface of the semiconductor substrate and partially on the sidewalls of the gate electrode; and

second spacers formed on the recessed spacers wherein the dielectric constant of the recessed spacers is greater than SiO_2 and the dielectric constant of the second spacers is less than the dielectric constant of the recessed spacers.

4. The semiconductor device according to claim 3, wherein third spacers are formed on the second spacers and the dielectric constant of the third spacers is less than the dielectric constant of the second spacers.

5. The semiconductor device according to claim 4, wherein the second spacers are L-shape and mirror L-shape.

6. A semiconductor device formed on a semiconductor substrate having an active region, the semiconductor device comprising:

a gate dielectric layer disposed on the semiconductor substrate;

a gate electrode formed on the gate dielectric layer defining a channel interposed between a source and a drain formed within the active region of the semiconductor substrate; and

graded dielectric constant spacers formed on sidewalls of the gate electrode, sidewalls of the gate dielectric layer and portions of an upper surface of the semiconductor substrate,

wherein the dielectric constant of the graded dielectric constant spacers decreases in value in a direction away from the gate dielectric.

7. The semiconductor device according to claim 6, wherein the graded dielectric constant spacers include:

a first layer formed on the sidewalls of the gate electrode, the sidewalls of the gate dielectric layer and the portions of the upper surface of the semiconductor substrate;

a second layer formed on the first layer;

a third layer formed on the second layer; and

a fourth layer formed on the third layer,

wherein the first layer has a dielectric constant greater than SiO_2 and each of the second, third and fourth layers has a dielectric constant less than the dielectric constant of the preceding layer.

8. The semiconductor device according to claim 7, wherein the first layer material is one or more of Al_2O_3, HfO_2, ZrO_2, Ta_2O_5, $BaTiO_3$, TiO_2, CeO_2, BST ($Ba_{1-x}Sr_xO_3$), PZN ($PbZn_xNb_{1-x}O_3$) and PST ($PbSc_xTa_{1-x}O_3$).

9. The semiconductor device according to claim 7, wherein the second layer material is one or more of SiO_2, Si_3N_4, SiO_xN_y, Al_2O_3, HfO_2, ZrO_2, Ta_2O_5, $BaTiO_3$, TiO_2, CeO_2, BST ($Ba_{1-x}Sr_xO_3$), PZN ($PbZn_xNb_{1-x}O_3$) and PST ($PbSc_xTa_{1-x}O_3$).

10. The semiconductor device according to claim 7, wherein the third layer material is one or more of SiO_2, Si_3N_4, SiO_xN_y, Al_2O_3, HfO_2, ZrO_2, Ta_2O_5, $BaTiO_3$, TiO_2, CeO_2, BST ($Ba_{1-x}Sr_xO_3$), PZN ($PbZn_xNb_{1-x}O_3$) and PST ($PbSc_xTa_{1-x}O_3$).

11. The semiconductor device according to claim 7, wherein the fourth layer material is one or more of SiO_2, Si_3N_4, SiO_xN_y, Al_2O_3, HfO_2, ZrO_2, Ta_2O_5, $BaTiO_3$, TiO_2, CeO_2, BST ($Ba_{1-x}Sr_xO_3$), PZN ($PbZn_xNb_{1-x}O_3$) and PST ($PbSc_xTa_{1-x}O_3$).

12. The semiconductor device according to claim 8, wherein the first layer is Al_2O_3.

13. The semiconductor device according to claim 9, wherein the second layer is Si_3N_4.

14. The semiconductor device according to claim 10, wherein the third layer is SiO_xN_y.

15. The semiconductor device according to claim 11, wherein the fourth layer is SiO_2.

16. A method of fabricating a semiconductor device formed on a semiconductor substrate having an active region, the method comprising the steps of:

forming a gate dielectric layer on the semiconductor substrate;

forming a source and a drain within the active region of the semiconductor substrate;

forming a gate electrode on the gate dielectric layer wherein the gate electrode defines a channel interposed between the source and the drain; and

forming graded dielectric constant spacers on sidewalls of the gate electrode, sidewalls of the gate dielectric layer and portions of an upper surface of the semiconductor substrate,

wherein the dielectric constant of the graded dielectric constant spacers decreases in value in a direction away from the gate dielectric layer.

17. The method according to claim 16, wherein the step of forming graded dielectric constant spacers further includes the steps of:

forming a first layer on the sidewalls of the gate electrode, the sidewalls of the gate dielectric and the portions of the upper surface of the semiconductor substrate;

forming a second layer on the first layer;

forming a third layer on the second layer; and

forming a fourth layer on the third layer,

wherein the first layer has a dielectric constant greater than SiO_2 and each of the second, third and fourth layers has a dielectric constant less than the dielectric constant of the preceding layer.

18. The method of claim 17, further including the step of:

forming the first layer of one or more of Al_2O_3, HfO_2, ZrO_2, Ta_2O_5, $BaTiO_3$, TiO_2, CeO_2, BST ($Ba_{1-x}Sr_xO_3$), PZN ($PbZn_xNb_{1-x}O_3$) and PST ($PbSc_xTa_{1-x}O_3$).

19. The method of claim 18, further including the step of:

forming the second layer of one or more of SiO_2, Si_3N_4, SiO_xN_y, Al_2O_3, HfO_2, ZrO_2, Ta_2O_5, $BaTiO_3$, TiO_2, CeO_2, BST ($Ba_{1-x}Sr_xO_3$), PZN ($PbZn_xNb_{1-x}O_3$) and PST ($PbSc_xTa_{1-x}O_3$).

20. The method of claim 19, further including the step of:

forming subsequent layers of one or more of SiO_2, Si_3N_4, SiO_xN_y, Al_2O_3, HfO_2, ZrO_2, Ta_2O_5, $BaTiO_3$, TiO_2, CeO_2, BST ($Ba_{1-x}Sr_xO_3$), PZN ($PbZn_xNb_{1-x}O_3$) and PST ($PbSc_xTa_{1-x}O_3$).